transistor. Incidentally, the construction of the low voltage PMOS and NMOS transistors are equal to those in the first embodiment.

IN THE CLAIMS

Please amend Claim 1 as shown in clean form below:[2]

1. (Amended) A semiconductor device, comprising:

a first transistor including a first gate formed on a semiconductor substrate, a first low impurity concentration diffusion layer formed on the surface of said semiconductor substrate in a manner to surround said first gate, a first high impurity concentration diffusion layer formed on the surface of the semiconductor substrate in a manner to surround said first low impurity concentration diffusion layer, and a first gate side wall formed to surround the first gate with a top surface of the first gate being exposed from an upper end of the first gate side wall, and an interface between the first low impurity concentration diffusion layer and the first high impurity concentration diffusion layer corresponding to a lower end of an outer surface of the first gate side wall; and

a second transistor including a second gate formed on the semiconductor substrate, a second low impurity concentration diffusion layer formed on the surface of the semiconductor substrate in a manner to surround said second gate, a second high impurity concentration diffusion layer formed on the surface of the semiconductor substrate in a manner to surround said second low impurity concentration diffusion layer, and a second gate side wall formed to surround said second gate and having a thickness equal to that of the first gate side wall of said first transistor, a top surface of the second gate being exposed from an upper end of the second gate side wall;

[2] A marked-up copy is attached hereto.